# Design and Development of Low actuation voltage RF MEMS switch using Elevated Coplanar Waveguides

*S.Kanthamani[1], Vamshi[2], K.N.Bhatt[3], S.Raju[4]*

[1] *Associate Professor, Department of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai-625015, India*
[2] *Research Scholar, Centre for Nano Science and Engineering(CeNSE), Indian Institute of Science, Bangalore, India.*
[3] *Emeritus Professor, Centre for Nano Science and Engineering(CeNSE), Indian Institute of Science, Bangalore, India.*
[4] *Professor, Department of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai-625015, India*
*E-mail: skanthamani@gmail.com*

A low actuation voltage Radio Frequency (RF) MEMS switch using Elevated Coplanar Waveguide (ECPW) is proposed and reported. A 20 GHz RF MEMS switch is designed, fabricated and characterized. The obtained pull-in of the proposed switch is 2-2.8 volts which is much lower in comparison to the conventional CPW switches. The measured RF performance of the switch shows an insertion loss of -2.7dB and a return loss of -11dB to -20 dB at 20 GHz and Mechanical resonant frequency was studied using Laser Doppler Vibrometer (LDV). The reduced pull in makes these switches suitable for high speed digital circuits.

**1. Introduction:** Micro Electro Mechanical switches are a proven solution for the development of RF MEMS circuits [1] which provides low loss, high isolation RF characteristics over a wide microwave frequency range. Various switch configurations such as rotary [2], cantilever [3-4], membrane structures are reported [5-7].

RF MEMS switches using metal membranes with capacitor coupling realized on CPW combines the advantages of MEMS technology and coplanar wave guide to achieve reduced size and better RF performance [8].The CPW switches show superior RF characteristics compared to solid state switches. However, as frequency increases, CPW switch suffers from dispersion loss caused by air- dielectric interface material discontinuity. The centre conductor width and gap width play a very important role in deciding the waveguide loss and bandwidth. They also determine the length of the bridge needed to realize a switch. The length of the switch in turn will decide the switch speed, isolation and insertion loss. Therefore in coplanar wave guide the constraints placed on conductor width and gap width has adverse impact on the final switch design. In addition, the ratio of capacitance during the ON and OFF states depends on the gap between signal line and bridge electrodes [9] requiring very high actuation voltage for operation upto 30volts.[10 ]. High actuation voltage causes high rate of dielectric charging and affects the life-time of a switch [11].

For monolithic microwave circuits, it is sufficient to have 5volts DC bias voltage for operation. In literature, many researchers have proposed different membrane configurations to lower the actuation voltage of the electrostatic type of RF MEMS switches[12-15].To overcome the performance constraints we have proposed a novel RF MEMS switch for low voltage operation. In section 2the proposed switch along with structural dimensions are presented. Section 3 gives the fabrication process flow of the proposed switch. Section 4 presents the characterization and results obtained with the fabricated device.

**2. Device Design:** The conventional RF MEMS CPW switch with capacitive coupling has been reported as shown in figure1(a), and the proposed novel RF MEMS switch realized on an ECPW platform in

shown in figure1(b). [14].The centre conductor of the proposed switch (figure 1b) is elevated by inserting a thin dielectric layer below the signal line. It also consists of a thin dielectric membrane above the signal line which gets connected to ground when actuated by a dc voltage which brings the switch to OFF state. In order to actuate the switch the centre conductor of the CPW line is biased with respect to the ground. The minimum potential required to actuate the switch is the pull-in voltage, $V_p$, which is given by the equation [1].

$$V_p = \sqrt{\frac{8kg_0^{\,3}}{27\varepsilon_0 A}} \qquad (1)$$

Equation (1) shows the dependency of actuation voltage on various parameters such as stiffness ($k$), the air-gap ($g_0$), and the overlapping area ($A$) between the electrodes of the switch. Therefore, in order to get a very low actuation voltage, the switch should have a low spring constant, $k$, and low air-gap. Here in the proposed switch by inserting a dielectric layer (h) of $\epsilon_{r2}$ below the central conductor, the signal carrying line is raised and hence the air gap between the electrodes gets reduced so that the pull in voltage also gets reduced. The dispersion characteristics caused by air- dielectric interface are diminished by elevating the signal line. [15]
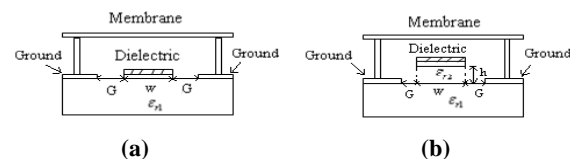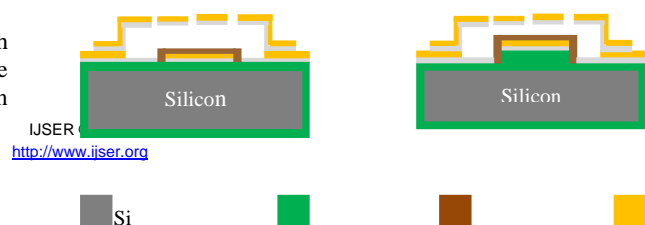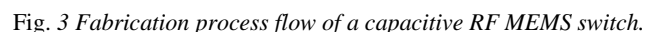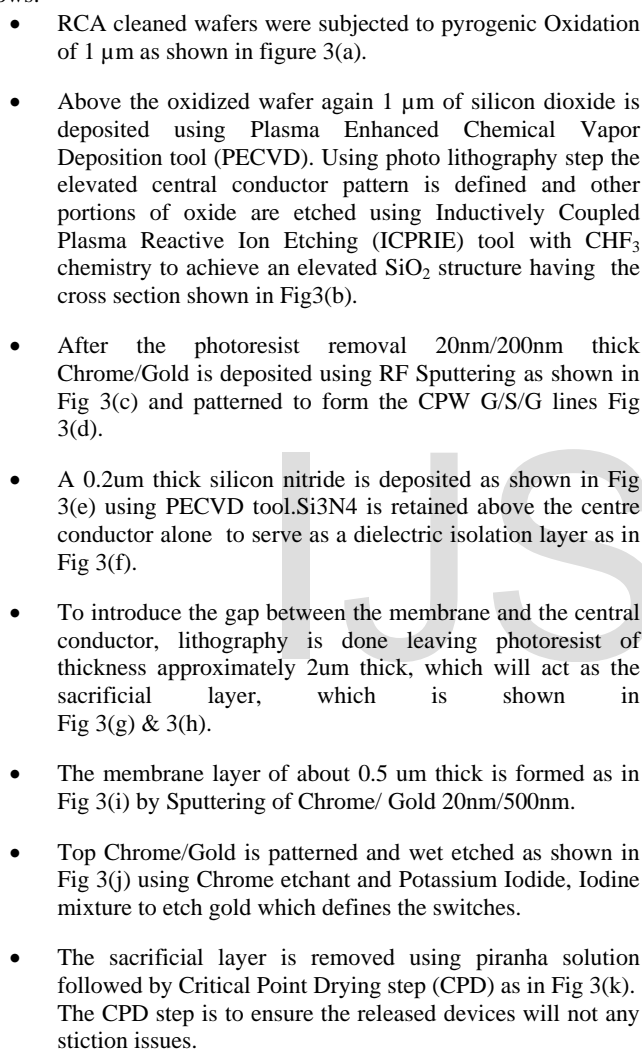


**(a)**       **(b)**

Fig. 1 *(a) Basic structure of conventional switch and (b) proposed switch.*

SiO₂              Si₃N₄              Cr/Au

**(a)**                            **(b)**

Fig. 2 *shows the cross section of conventional switch (a) and proposed switch (b)*

## 3. Fabrication Process:

The proposed switch was fabricated on a 475 - 500 µm silicon substrate with resistivity 1-100 ohm-cm. The fabrication steps are as follows:

- RCA cleaned wafers were subjected to pyrogenic Oxidation of 1 µm as shown in figure 3(a).

- Above the oxidized wafer again 1 µm of silicon dioxide is deposited using Plasma Enhanced Chemical Vapor Deposition tool (PECVD). Using photo lithography step the elevated central conductor pattern is defined and other portions of oxide are etched using Inductively Coupled Plasma Reactive Ion Etching (ICPRIE) tool with $CHF_3$ chemistry to achieve an elevated $SiO_2$ structure having the cross section shown in Fig3(b).

- After the photoresist removal 20nm/200nm thick Chrome/Gold is deposited using RF Sputtering as shown in Fig 3(c) and patterned to form the CPW G/S/G lines Fig 3(d).

- A 0.2um thick silicon nitride is deposited as shown in Fig 3(e) using PECVD tool.Si3N4 is retained above the centre conductor alone to serve as a dielectric isolation layer as in Fig 3(f).

- To introduce the gap between the membrane and the central conductor, lithography is done leaving photoresist of thickness approximately 2um thick, which will act as the sacrificial layer, which is shown in Fig 3(g) & 3(h).

- The membrane layer of about 0.5 um thick is formed as in Fig 3(i) by Sputtering of Chrome/ Gold 20nm/500nm.

- Top Chrome/Gold is patterned and wet etched as shown in Fig 3(j) using Chrome etchant and Potassium Iodide, Iodine mixture to etch gold which defines the switches.

- The sacrificial layer is removed using piranha solution followed by Critical Point Drying step (CPD) as in Fig 3(k). The CPD step is to ensure the released devices will not any stiction issues.

**(c)**                            **(d)**

Si3N4                            Si3N4 Etch

**(e)**                            **(f)**

Litho mask (AZ5214E (2.2µm))        Litho mask (PR )

**(g)**                            **(h)**

Sputtered Cr/Au (50 nm/500 nm)      Cr /Au wet etch

**(i)**                            **(j)**

Release (CPD)

**(k)**

Fig. *3 Fabrication process flow of a capacitive RF MEMS switch.*

**4. Testing and Measurement:** The proposed switch was fabricated and validated in the National Nano Fabrication Centre at the Centre for Nano Science and Engineering, Indian Institute of Science, Bangalore India. In figure 5 the airgap can be seen which indicates the switch is released and is not having any stiction issues. As shown in SEM image and optical profiler of the proposed switch of the figure 4 and 6, the switch was fabricated on ECPW platform with dimensions of G/W/G = 60/100/60 for DC - 20 GHZ measurements on silicon substrate. The membrane length is 215 µm. The membrane height is $g_0$ = 2 µm and the membrane thickness is 0.5 µm. The height of the inserted dielectric layer is 1 µm.

**SiO₂ (1 µ m)**                   **Elevated SiO₂**

**(a)**                            **(b)**

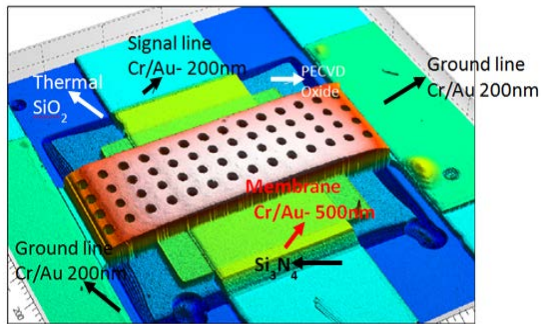**Sputtered Cr/Au (20nm/200nm)**   **Cr /Au etch**

Fig. *4. 3D Optical Profiler image of the device*
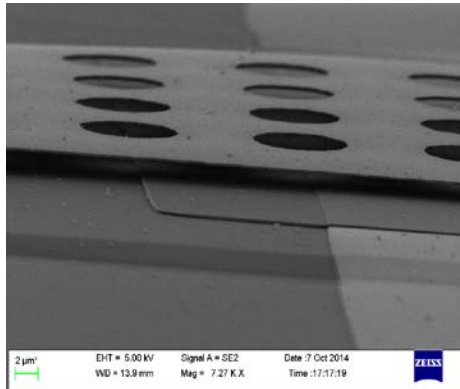


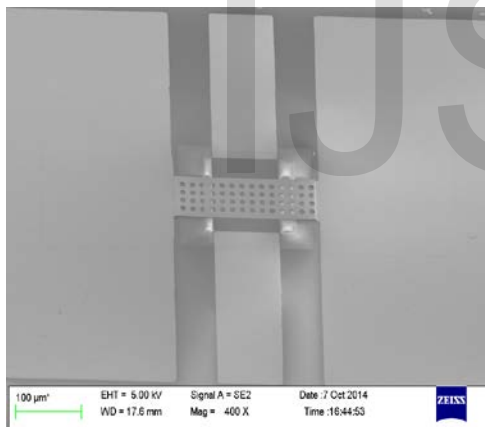Fig. 5 *Released membrane with air gap and the inserted dielectric*



Fig. 6 *SEM image of the fabricated ECPW switch*
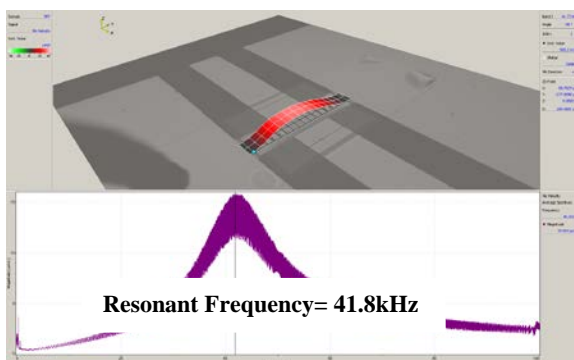


**Resonant Frequency= 41.8kHz**

Fig. 6 *Mechanical resonant frequency response using LDV*
Vibration measurement of the membrane resulting in generation of various modal shapes and mechanical resonant

frequency was studied using Laser Doppler Vibrometer (LDV). The frequency response of the switch due to 3 V DC and 0.8 V AC is shown in Fig. 7. The extracted resonant frequency, $f0$, from this response is found to be 41.8 kHz as the first natural frequency.

The scattering parameters of the proposed switch was done using Cascade Microtech Summit 9000 Probe station interfaced with Agilent E8361A Performance Network Analyzer on wafer coplanar probes with 200 µm pitch from 0.01 GHZ to 20 GHZ as shown in figure 8 . When the switch is in the UP state an insertion loss of -2.7dB at 20 GHZ with a return loss of -11dB was measured.When the switch is in the DOWN state an isolation better than -5.7dB at 20 GHZ was measured. The reason for the low isolation could be due to the amorphous PECVD oxide used in the current process, if the quality of oxide is improved we believe that the isolation will be better. A comparison of the simulated and measured radio frequency results are presented in Table I and figure 8. These results are found to be in close agreement.

**Table 1: Simulated and experimental results of the proposed switch**

| SWTICH TYPE | PULL - IN VOLTAGE (V) | UPSTATE | | | | DOWNSTATE | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | SIMULATED | | MEASURED | | SIMULATED | | MEASURED | |
| | | S11 (dB) | S12 (dB) | S11 (dB) | S12 (dB) | S11 (dB) | S12 (dB) | S11 (dB) | S12 (dB) |
| ECPW | 2 - 2.8 | -5.18 | -2.34 | -22 | -2.2 | -2.45 | -4.92 | -21 | -5 |
| CPW | 7 - 8 | -14.08 | -0.57 | -29 | -1.9 | -5.75 | -2.2 | -14 | -2.5 |
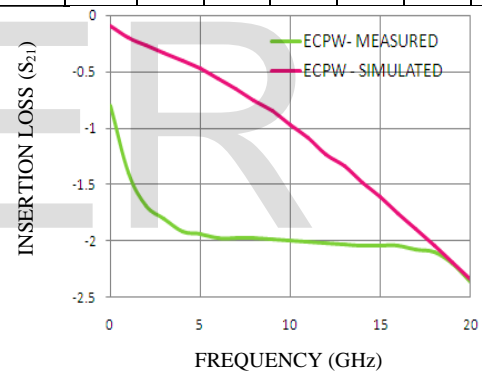


**(a)**
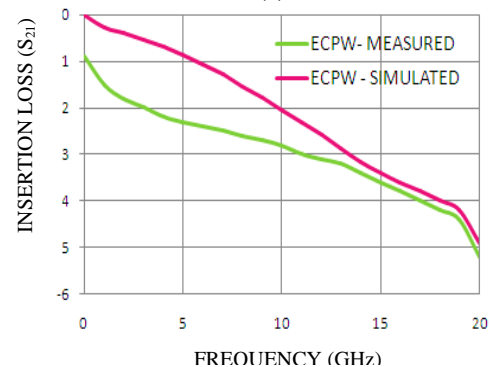


**(b)**

Fig. 7 *Measured S-parameters in UP- state (a) and DOWN-state (b) positions*

On an average the actuation voltage is 2 - 2.8 volts. Since the gap height between the centre conductor of ECPW and membrane is

reduced, the pull in voltage gets reduced. The measured Capacitance in the UP and DOWN states are 1.18 pF and 935 pF respectively.

**5. Conclusion:** A novel ECPW shunt switch is proposed in this paper. The switch has been designed, fabricated and reported for low actuation voltage. Mechanical and RF performance of the proposed switch is measured. The pull down voltage of the proposed switch is around 2- 2.8 volts with a compromise in the isolation of the switch. Since the gap height gets reduced in the ECPW switch due to insertion of dielectric layer, the pull-in voltage is reduced as compared to the conventional CPW switches, making it as a suitable candidate for high speed digital interconnect applications.

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